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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,474	07/18/2003	Paolino Schillaci	856063.743	4573

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,474	SCHILLACI ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 17-20* is/are pending in the application.

4a) Of the above claim(s) *14-16* is/are withdrawn from consideration.

5)☒ Claim(s) *17-20* is/are allowed.

6)☒ Claim(s) *1,2,7 and 11-13* is/are rejected.

7)☒ Claim(s) *3-6 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed May 03, 2006. This amendment has been entered and carefully considered. Claims 1-13 and 17-20 remain pending in the application. Claims 14-16 have been canceled. Claims 17-20 are allowable.

2. Applicant's arguments filed May 03, 2006 with respect to claims 1, 2, 7 and 11-13 have been fully considered but they are not deemed to be persuasive.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 7 and 11-13 are rejected under 35 U.S.C. § 102(b) as being anticipated by Shiau et al. (USPN: 6,119,226); hereinafter Shiau.

As per claim 1, Shiau discloses the invention as claimed including an automatic decoding method for mapping and selecting a nonvolatile memory device having a LPC serial communication interface, wherein the memory is equipped with a plurality of addressing pins and mounted on a motherboard together with other memories of the same type bidirectionally connected with a controller putting it into communication with a processor housed in turn on the motherboard (e.g. see abstract, column 2, lines 29 et seq. and figure 1) comprises a processor that compares the addressing pins of each memory with a portion of the addressing coding bits both to identify the addressing type to be used, top-down or bottom-up, and to determine which memory is polled by the controller for a given operation; for example, Shiau discloses the decoders for decoding address coding bits by inverting the high order address bits to identify whether the memory access request is in the first type or second type address protocol and to determine which memory array row in the first type is polled for certain operation (e.g. see column 5, lines 27 et seq., column 10, lines 1-12);

As per claim 2, wherein the comparison is performed in a LPC decoding block (e.g. see column 2, lines 22 et seq.; column 10, lines 7-12).

As per claim 7, Shiau discloses a non-volatile memory integrated device equipped with an interface with LPC serial protocol and a plurality of addressing pins in order to be mounted on a motherboard together with other memories of the same type bidirectionally connected with a controller putting it into communication with a processor housed in turn on the motherboard (e.g. see column 2, lines 29 et seq.; column 6, lines 25 et seq.) wherein the processor contains in the LPC interface a logic identification structure both of the memory and of the addressing type to be used, top-down or bottom-up (e.g. see column 2, lines 38 et seq.); and the logic structure contains a comparator to compare a portion of the addressing coding bits with the addressing pins; for example, Shiau discloses the decoders for decoding address coding bits by inverting the high order address bits to identify whether the memory access request is in the first type or second type address protocol and to determine which memory array row in the first type is polled for certain operation; Shiau clearly discloses the logic is located within the decoder to decode a memory access request for boot code to the appropriate location in the array (e.g. see column 2, lines 58-64; column 5, lines 27 et seq., column 10, lines 1-12);

As per claim 11, it encompasses the same scope of invention as to that of claims 1 and 7 except that it is drafted as method format rather than apparatus format, the claim is therefore

rejected for the same reasons as being set forth above. Noting that the further limitation of addressing particular locations within selected memory circuit with either top-down or bottom-up using second set of addressing pins is taught by Shiau; for example, Shiau discloses the decoders in his memory system decode a memory access request to select a row of the memory array, and the control has an output for outputting either a bottom-up or a top-down address protocol signal through particular set of pin of input pins wherein his integrated circuit memory having a plurality of address, and including a memory array having multiple memory circuits with plurality of rows and columns of memory cells. The inputs connect to a corresponding one of the address input pins, and wherein outputs connect to a corresponding row of the memory array. (e.g. see column 2, lines 29 et seq.; also see column 3, lines 44 et seq.).

As per claims 12 and 13, the further limitation of sending a reset pulse if the identification signals do not indicate a unique decoding scheme and there is not a direct match between the enabling signal and the bits residing on addressing pins of the memory circuit is taught by Shiau as addresses received from a processor implementing a T-type protocol will not be converted and therefore address protocol unit 136 output a logic 0 level

signal (e.g. see column 7, lines 46 et seq.);

Allowable subject matter

5. Claims 17 and 18 are allowed. Claims 19-20 are dependent of claim 18, they are also allowable. Claims 3 and 8 are objected to as being dependent upon a rejected base claims 1 and 7 respectively, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. Claims 4-6 and 9-10 are also allowable since they are dependent upon the indicated allowable claims 3 and 8.

6. As per remark, Applicant's counsel argued that the prior art of Shiau does not discuss selecting a memory from a plurality of memories as being claimed (amendment's page 7, third paragraph). First of all, it should be noted that Shiau clearly discloses that his integrated circuit memory includes plurality of memory blocks/cells of memory array wherein in memory cells/blocks can be selected based on different top-down or bottom-up selecting scheme (e.g. see column 2, lines 38 et seq., and abstract) wherein the memory blocks/cells is considered to be well equivalent to the "memory" as being contended by Applicant's counsel.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the

extension of time policy as set forth in 37 C.F.R. . 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. . 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on

access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/July 20, 2006

Tuan V. Thai
PRIMARY EXAMINER
Group 2100